Remarks

In the Final Office Action dated November 25, 2009, the following rejections were indicated: claims 1, 2, 5, 6, 14-16 and 21 were rejected under 35 U.S.C. § 103(a) over Krishnamurthy (U.S. Patent No. 6,233,178) in view of Iwahashi (U.S. Patent No. 4,247,918); claims 3, 7-9, 11, 17 and 20 were rejected under 35 U.S.C. § 103(a) over the '178 reference in view of the '918 reference further in view of Guliani (U.S. Patent No. 6,366,497); claims 4 and 10 were rejected under 35 U.S.C. § 103(a) over the '178 reference in view of the '918 and '497 references and further in view of Takahashi (U.S. Patent No. 6,639,849); and claims 12-13 and 18-19 were rejected under 35 U.S.C. § 103(a) over the '178 reference in view of the '918 and '497 references and further in view of Kurihara (U.S. Patent Pub. 6,791,880). Applicant respectfully traverses all claim rejections, and in this discussion set forth below, does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

Applicant appreciates the Examiner's time in discussing the instant claims via telephone. Based upon these conversations and this paper, Applicant believes that the claims should be in condition for allowance. Should any issues remain, Applicant invites a telephone call to the undersigned. The following addresses the rejections and the believed appropriateness of Applicant's traversals of record, and further discusses amendments as made herein, to facilitate prosecution.

The § 103 rejection of claims 1, 2, 5, 6, 14-16 and 21 relies upon an erroneous assertion that the cited floating gate is the same as a charge trapping device. This assertion is improper because the cited floating gate does not and cannot operate in accordance with a charge trapping device as claimed. The Office Action's attempt to equate these very different devices with one another contradicts both Applicant's specification and well-documented operation of a floating gate, contrary to M.P.E.P. § 2111.01.

Specifically, a floating gate permits lateral charge transport within the floating gate layer, and relies upon an external component (*e.g.*, dielectric layers) to maintain charge. In contrast and as consistent with page 1:10-22 of Applicant's specification, a charge-trapping layer actually functions to trap charge within the layer, such as by trapping charge in energy minima of a charge-trapping layer. In other words, while

charge can be confined to a floating gate using external materials to prevent lateral charge transport out of the floating gate, a floating gate as asserted cannot trap charge and thus cannot be interpreted as functioning in accordance with a "charge trapping device" as claimed. This is also consistent with the '178 reference, which fails to even mention the term "trap." For reference, Applicant refers to page 1:19-21 of the instant specification, which describes contrasting properties of charge-trapping devices and floating-gate devices as follows:

> In a FG device, lateral charge transport is possible inside the FG layer, which is not the case in a charge trapping device: there the charge is trapped at a substantially fixed location inside the charge trapping layer.

As consistent with the above, the cited floating gate does not trap any charge, as the charge is free to move via lateral transport in the floating gate. As consistent with M.P.E.P. 2111.01, claim terms cannot be given such meaning when it is "inconsistent with the specification" (citing *Chef America, Inc. v. Lamb-Weston, Inc.*, 358 F.3d 1371, 1372 (Fed. Cir. 2004)), and such terms must be given a "reasonable" interpretation that must be made "in light of the specification."

In view of the above, Applicant believes the rejections are improper and maintains its traversals of record. To facilitate prosecution, Applicant has amended each independent claim in a manner that is believed to be consistent with respective claims, prior to amendment, relative to the trapping of charge within a charge-trapping layer. Applicant believes that this amendment should assist the Examiner in understanding the lack of correspondence in the cited floating gate devices, which is further consistent with Applicant's specification as discussed above (which further supports these amendments). The cited references thus fail to correspond to a charge trapping layer and methods for the same as in the independent claims. Applicant therefore requests that the rejections be removed.

In view of the above, further discussion of the rejections is believed inapplicable. However, Applicant has addressed certain traversals below, as generally consistent with those as presented in the record and incorporated herein.

The § 103 rejection of claims 1, 2, 5, 6, 14-16 and 21 also fails to establish correspondence to the respective limitations directed to programming and erasing memory cells, because the cited logical "1" and "0" in the Iwahashi reference represent

two different logical interpretations of the same signal, thus failing to correspond to charge and discharge states as asserted. According to Iwahashi, a charge state could represent a logical "1" and a discharge state could represent a logical "0" in a first implementation, and in a second implementation, a charge state could represent a logical "0" and a discharge state could represent a logical "1." In either case, the underlying memory device is unchanged, as switching logical ones or zeroes does not change the underlying charge states and function of the device. The required erasure and programming step for a write operation does not change simply because the logical values are swapped. Thus, the device of the '918 reference would still perform block erasures in the exact same manner (relative to charge and discharge states) regardless of how logical ones or zeroes are assigned. Accordingly, Applicant submits that the rejection is erroneous and requests that it be reversed.

Applicant further maintains that modifying the '178 reference as proposed in the Office Action (or as required to arrive at the claimed invention) is improper because the '178 reference would be inoperable for its stated purpose if so modified. As consistent with the M.P.E.P. and relevant case law, if a "proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *See* M.P.E.P. 2143.01, citing *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984). Specifically, the '178 reference expressly teaches that the problem being addressed by the '178 reference is due to excess charge buildup. In addressing this problem, the stated purpose of the '178 reference is to precondition memory cells before an erasure ever occurs to specifically avoid charging an already charged cell. The '178 reference explains that this is done to mitigate stress buildup due to erasures (Col. 5:39-40). The Examiner's proposed modification of the '178 reference would result in charging already charged cells, which directly contradicts the stated purpose of the '178 reference and renders it inoperable. As such, it is impermissible to modify the '178 reference in a manner that defeats the express and primary purpose of avoiding charging already charged cells.

Applicant further submits that the '178 reference also teaches away from the claimed invention, including aspects directed to a floating gate (that explicitly does not trap charge, but rather permits lateral charge transport), as well as others, thus rendering

the § 103 rejection of claims 1, 2, 5, 6, 14-16 and 21 improper. More particularly, the M.P.E.P. and applicable law requires that the claims be considered "as a whole" (35 U.S.C. §103(a)), while taking into consideration the problem(s) being addressed by the claimed invention and any unexpected results. The Supreme Court in *KSR*[1] reaffirmed the familiar framework for determining obviousness as set forth in *Graham v. John Deere Co.* (383 U.S. 1, 148 USPQ 459 (1966)), and stated that, "when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious." The Court further tied in the relationship between the teach-away standard and demonstrating unpredictable results. "The fact that the elements [in *Adams*] worked together in an unexpected and fruitful manner supported the conclusion that Adam's design was not obvious to those skilled in the art."

As applicable here, the '178 reference expressly teaches that the problem being addressed by the '178 reference is due to excess charge buildup. Thus, the proposed combination, based upon the primary '178 reference, not only fails to correspond to the claimed invention, it also expressly teaches that charging is a problem to be avoided. Accordingly, since the '178 reference teaches a memory management approach that causes the problems noted in the background of the instant application, the reference actually teaches away from the asserted combination of references, and further from the claimed invention itself. Applicant therefore maintains that the rejection is improper.

Applicant further maintains that the § 103 rejection of claims 1, 2, 5, 6, 14-16 and 21 is also improper because no evidence has been provided in support of the allegedly inherent functions. "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" M.P.E.P. § 2112 citing to *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999) (citations omitted). Thus, the existence of a single implementation that does not correspond to the alleged inherent aspect invalidates any argument of inherency. As applicable here, the rejection relies upon allegations of inherency relating, for example, to claim limitations directed to

[1] *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (U.S. 2007)

specific sequences of programming and erasure. However, the primary '178 reference does not respond to a block erase request by programming before erasure, or otherwise to the limitations as claimed. This sequence of programming and erasure is not inherent, because the erasure could be (and is taught to be) implemented without first programming. Accordingly, the Examiner has failed to establish that the '178 reference necessarily operates as suggested, rendering the § 103 rejection *prima facie* invalid. Applicant therefore maintains its traversals.

Applicant submits that the § 103 rejection of claims 3, 7-9, 11, 17 and 20 is improper for reasons including those discussed above in connection with each of the independent claims, and is also improper because it fails to establish that the cited reference cell in the '497 reference corresponds as asserted. The cited portion of the '497 reference simply teaches that a reference cell can be used for programming or erasing configurations. However, it does not teach that the reference cell is actually programmed and erased for a block-programming and block-erasing of the non-volatile memory devices in the array. This lack of correspondence is further relevant to the above-discussed lack of correspondence in the cited floating gate, relative to a charge-trapping layer. Specifically regarding the rejection of claim 20, this rejection is also improper for failing to provide evidence in support of the allegedly inherent functions, which is improper as discussed above. Applicant therefore maintains its traversals of the § 103 rejection of claims 3, 7-9, 11, 17 and 20.

Applicant submits that the rejection of claims 4 and 10 is improper for reasons including those discussed above in connection with independent claims 1 and 5. The rejection of claims 4 and 10 is further improper because it fails to establish that the alleged motivation ("judging a level of read data") would be pertinent to the combination at hand, and/or relevant to the actual modification of the primary '178 reference. Moreover, this alleged motivation does not appear to directly apply to any motivation relevant to the claim limitations at hand, namely, "memory devices of the array" that "function as reference cells." Accordingly, Applicant maintains its traversals of the § 103 rejection of claims 4 and 10.

Applicant submits that the rejection of claims 12-13 and 18-19 is improper for reasons including those discussed above in connection with independent claims 5 and 16.

Applicant submits that the rejections are further improper, as follows. The rejection of claim 12 is improper because it fails to establish that the alleged motivation ("providing current after aging") would be pertinent to the combination at hand, and/or relevant to the actual modification of the primary '178 reference (*e.g.*, that the '178 reference would benefit from such current provision) as this alleged motivation is stated only as beneficial to the secondary '880 reference. The rejection of claims 13 and 18-19 also fail because as the Office Action has provided no motivation for combining references as asserted. Specifically, pages 12 and 13 of the Final Office Action appear to allege correspondence, but fail to mention any motivation for modifying the '178 reference to include the allegedly corresponding disclosure in the secondary '880 reference. Accordingly, Applicant maintains its traversals regarding the rejections of claims 12-13 and 18-19.

In view of the above, Applicant believes that each of the rejections is improper and/or no longer applicable, and that the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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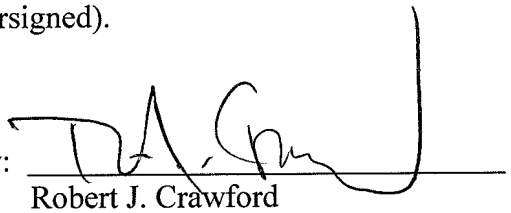
By: 

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